REMARKS

Claims 32, 33, 35, 37, 38 and 47-55 were previously pending in the present application. Claims 32, 35, 37, 49, 51 and 52 are amended as set forth above. Claims 48 and 55 are canceled. Reconsideration of this application and allowance of each of presently pending claims 32, 33, 35, 37, 38, 47 and 49-54 is respectfully requested.

Amendments of Claims 32, 35, 37, 49, 51 and 52

Claims 32 and 49 have been amended to incorporate distinguishing features that appeared in Claims 48 and 55, respectively, which are canceled in this response. Claims 48 and 55 are canceled without prejudice.

Claims 37 and 52 have been amended for consistency with the amendments made to Claims 32 and 49, respectively.

Claims 35 and 51 have been amended to more particularly point out distinguishing features of the claims. No new matter is added.

Objection to Drawings

The Action objects to the drawings under 37 CFR §1.83(b) as being incomplete. Specifically, the Examiner alleges that the illustration of the invention is incomplete through failure to identify the claimed multiple bipolar transistors in cross-sectional view. As set forth above, Claims 32 and 49 have been amended, deleting the feature of "multiple bipolar transistors." Further, remaining Claims 33, 35, 37, 38, 47, 48 and 50-55 do not recite the feature of "multiple bipolar transistors," either. Withdrawal of the drawings objection is respectfully requested.

Objection to Claims

The Action objects to Claims 32-33, 35, 37-38, 47-48 and 49-55 and contends that the claim includes the informalities of: "a top one of said first regions" and "a bottom one of said second regions." Claims 48 and 55 are canceled and the objection of Claims 48 and 55 is thus

obviated. Claims 32 and 49 have been amended as set forth above in response to the Examiner's suggestion.

The Action also objects to Claims 32-33, 35, 37-38, 47-48 and 49-55 for the following claim informality: "with "N" number of said third regions, whereby "N" is the number of multiple bipolar transistors." Claims 48 and 55 are canceled and the objection of Claims 48 and 55 is thus obviated. Since the feature of: "whereby "N" is the number of multiple bipolar transistors" has been deleted from claim 32 according to the Examiner's suggestion, withdrawal of the objection to the claims is respectfully requested.

Claim rejections under 35 U.S.C. §102(b)

The Action rejects and contends Claims 32-33, 37-38, 47-50 and 52-55 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,850,095 to Chen et al. ("Chen"). Applicant submits that Claims 32-33, 37-38, 47-50 and 52-55 are not anticipated by Chen in view of the amendments set forth above and the arguments set forth below.

Claims 48 and 55 are canceled and the rejection of Claims 48 and 55 is thus moot.

Claim 32 has been amended to recite that

"... wherein said third regions are alternatingly arranged in an array within said third semiconductor layer, wherein, when "N" by definition is the number of said third regions, said third regions are electrically connected by a conductor element to N horizontal stripe conductor elements, and at least two of said horizontal stripe conductor elements are connected by at least one first contact conductor element horizontally perpendicular to said horizontal stripe conductor elements at one end of said horizontal stripe conductor elements, and at least two of said horizontal stripe conductor elements are connected by at least one second contact conductor element horizontally perpendicular to said horizontal stripe conductor elements at another end of the horizontal stripe conductor elements so that said horizontal stripe conductor elements are electrically connected to each other; ...."

In short, the number of the third regions is equal to the number of the horizontal stripe conductor elements which are electrically connected together.

Chen is directed to an ESD protection circuit using a zener diode. Chen states that the high efficiency ESD protection circuit 40 has a "four" emitter NPN structures as shown in FIG. 4, Col. 3, Lines 27 – 29. Referring to Chen's FIG. 4, the ESD protection circuit 40 includes "five" n+ regions 66. However, only "four" of them are electrically connected to each other via emitter polysilicon regions 68 to ground (the central n+ region 66 is coupled to pad 34 via polysilicon region 68, serving as Zener diode 80). In other words, the number (5) of n+ regions 66 is not equal to the number (4) of the polysilicon regions 68, which are electrically connected to a same voltage. It is submitted that Chen fails to teach or suggest the claimed feature of the third regions being connected to a corresponding number of horizontal stripe conductor elements.

Further, Chen in his specification states that the ESD circuit of the present invention provides a higher efficiency, more space efficient ESD circuit that is achieved through uniform turn-on of multi-emitter fingers from an internal Zener diode 80. Zener diode 80 must be coupled to a voltage source which is different from that of emitter NPN structures as shown in FIG. 4, or Chen's intended ESD circuit cannot be achieved. Accordingly, one of ordinary skill in the art, in possession of Chen, would not have been motivated to electrically connect Zener diode 80 with emitter NPN structures as would be required to achieve the feature recited in Claim 32.

Finally, Claim 32 has been amended to recite

"... at least two of said horizontal stripe conductor elements are connected by at least one first contact conductor element horizontally perpendicular to said horizontal stripe conductor elements at one end of said horizontal stripe conductor elements, and at least two of said horizontal stripe conductor elements are connected by at least one second contact conductor element horizontally perpendicular to said horizontal stripe conductor elements at another end of the horizontal stripe conductor elements so that said horizontal stripe conductor elements are electrically connected to each other; ...." (Emphasis added).

In the Action, Examiner referred to the indented portion of polysilicon region 68 of Chen as a horizontal stripe conductor element recited in Claim 32, and the contact between n+ region 66 and polysilicon region 68 as the first contact conductor element. However, Chen's contact between n+ region 66 and polysilicon region 68 is not horizontally perpendicular to the indented portion of polysilicon region 68. In addition, nothing in the description or drawings of Chen discloses or suggests the claimed features.

Based on the foregoing, it is submitted that Claim 32 is not anticipated by Chen and is, therefore, distinguished from Chen and allowable for at least the reasons set forth above.

Claims 33, 37-38 and 47 depend from Claim 32 and are, therefore, also allowable over the art of record.

Claim 49 has been amended to recite

> " . . . a number of the second n+-type regions is represented by "N," whereby the second n+-type regions are electrically connected by a conductor element with N horizontal stripe conductor elements, and at least two of said horizontal stripe conductor elements are connected by at least one first contact conductor element horizontally perpendicular to said horizontal stripe conductor elements at one end of said horizontal stripe conductor elements, and at least two of said horizontal stripe conductor elements are connected by at least one second contact conductor element horizontally perpendicular to said horizontal stripe conductor elements at another end of said horizontal stripe conductor elements so that said horizontal stripe conductor elements are electrically connected to each other; . . . ."

As the reasons argued above in connection with Claim 32, Claim 49 is not anticipated by Chen and is, therefore, allowable for at least the reasons set forth above.

Claims 50 – 54 depend from Claim 49 and are, therefore, allowable over the art of record for at least the reasons set forth above.

Reconsideration and withdrawal of the §102(b) rejections are respectfully requested.

Conclusion

In view of the foregoing amendments and remarks, Applicant submits that this application is in condition for allowance. Early notification to that effect is respectfully requested.

The Commissioner for Patents is hereby authorized to charge any additional fees or credit any excess payment that may be associated with this communication to deposit account **04-1679.**

Respectfully submitted,

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